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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/688,897	10/21/2003	Mitsuhiro Watanabe	Okl.592	3759

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EXAMINER	
GELAGAY, SHEWAYE	
ART UNIT	**PAPER NUMBER**
2137	

MAIL DATE	DELIVERY MODE
10/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/688,897	WATANABE, MITSUHIRO	
	Examiner	Art Unit	
	Shewaye Gelagay	2137	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) *4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group 1 (claims 1-3) in the reply filed on August 24, 2007 is acknowledged. Claim 4 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected claim.

2. Claims 1-3 are pending.

Response to Arguments

3. Applicant's arguments filed April 25, 2007 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Art (hereinafter Admission) in view of Matsumoto U.S. Patent Number 5,657,330.

As per claim 1:

Admission teaches a microcomputer comprising:

a first memory where a normal-operation program is stored; (figure 2, item 2)

a second memory where a functional test program stored; (figure 2, item 3)

a test mode detection circuit which monitors a signal supplied through an external terminal and detects if a test mode is designated; (figure 2, item 9)

a central processing unit (CPU) which accesses said first memory and runs said normal-operation program when said test mode is not designated, and accesses said second memory and runs said functional test program when said test mode is designated; (figure 2, item 1)

a memory management unit which monitors an access address and data with respect to said first and second memories and causes said CPU to execute a specific operation when there has been an unauthorized illegitimate access; (figure 2, item 7; page 3, line 25-page 4, line 3) and

a test circuit which gives a preset specific instruction to said CPU when, in said test mode, a specific memory area has been accessed. (figure 2, item 8; page 4, line 4-page 5, line 13; the test circuit gives test instruction to the CPU from the test signal...test instructions are given to the test signal input terminals of the test circuit and the CPU is allowed to execute a sequence of arbitrary instruction to test if the CPU cn properly execute the application program)

Admission does not explicitly disclose a security test signal has been output from said CPU and a specific memory area has been accessed. Matsumoto in analogous art, however, discloses a security test signal has been output from said CPU and a specific memory area has been accessed. (col. 13, lines 51-58) Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the

method disclosed by Admission with Matsumoto in order to provide a test mode signal output means for outputting the test mode signal. (Abstract; Matsumoto)

As per claim 2:

The combination of Admission and Matsumoto teaches all the subject matter as discussed above. In addition, Admission further discloses a microcomputer wherein said specific instruction given to said CPU from said test circuit is a instruction which is to be detected by said memory management unit as an illegitimate access. (page 4, line 4-page 5, line 13)

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Art (hereinafter Admission) in view of Takagi U.S. Patent Number 5,280,618.

As per claim 3:

Admission teaches a microcomputer comprising:

a first memory where a normal-operation program is stored; (figure 2, item 2)

a second memory where a functional test program stored; (figure 2, item 3)

a test mode detection circuit which monitors a signal supplied through an external terminal and detects if a test mode is designated; (figure 2, item 9)

a central processing unit (CPU) which accesses said first memory and runs said normal-operation program when said test mode is not designated, and accesses said second memory and runs said functional test program when said test mode is designated; (figure 2, item 1)

a memory management unit which monitors an access address and data with respect to said first and second memories and causes said CPU to execute a specific operation when there has been an unauthorized illegitimate access; (figure 2, item 7; page 3, line 25-page 4, line 3) and

a circuit, for executing a predetermined exception process when said functional test program is executing a security test and said memory management unit has instructed execution of said specific operation. (figure 2, item 8; page 4, line 4-page 5, line 13; the test circuit gives test instruction to the CPU from the test signal...test instructions are given to the test signal input terminals of the test circuit and the CPU is allowed to execute a sequence of arbitrary instruction to test if the CPU cn properly execute the application program)

Admission does not explicitly disclose an exception processing circuit, included in said CPU. Takagi in analogous art, however, discloses an exception processing circuit, included in said CPU. (figure 1; col. 2, line 51-col. 3, line 11) Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the method disclosed by Admission with Takagi in order to facilitate interrupt performance tests by carrying tests independently and precisely with the minimum time and procedure. (col. 2, lines 55-60; Takagi)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shewaye Gelagay whose telephone number is 571-272-4219. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on 571-272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Shewaye Gelagay SG

EMMANUEL L. MOISE
SUPERVISORY PATENT EXAMINER